

REMARKS

Claims 1-27 are rejected under 35 USC §112, first paragraph, as not being supported by the application as filed. Furthermore, claims 12 and 34 are rejected under 35 USC §112, second paragraph as being indefinite.

Claims 28-33 and 35-39 are allowed. Claims 1, 12, and 34, and thus the remaining claims, would be allowable if amended to overcome the 35 USC §112 rejections.

The Examiner's rejections are respectfully traversed.

Before describing the essence of the invention, the problem that the invention addresses will first be briefly described.

The invention is directed towards the formation of a multi-layer semiconductor device in which components, typically, a micro-mechanical component or components are formed in one of the semiconductor layers, which normally would be a silicon layer. The silicon layer in which the components are formed is located between two outer layers, which would also normally be silicon layers. It should be noted that the invention is not concerned with the formation of components in the two outer layers, since there are many prior art methods for forming components in the outer layers of a multi-layer semiconductor device. Thus, it is emphasized that the invention is directed towards the formation of a multi-layer semiconductor device in which the components are formed in an inner layer, in other words, a layer which is located intermediate or between the two outer layers. Furthermore, and most importantly, the invention is directed towards the formation of the components in the inner layer after all the layers have been bonded together.

One advantage of the invention is that the micro-mechanical components in the inner layer are not subjected to the high temperatures which are required in anneal bonding, which is used in the bonding of the layers of the multi-layer semiconductor device together, since the micro-components are formed after bonding of the layers. This is an important advantage, since micro-mechanical components in general are sensitive components, and in particular, are sensitive to the high temperatures of anneal bonding, and are prone to damage by such high temperatures, and indeed, are also prone to damage resulting from the normal handling of the layers when the multi-layer structure is being formed.

In prior art methods, if micro-mechanical components were to be accurately formed in an inner layer of a multi-layer semiconductor structure, the micro-mechanical components would have to be formed in the inner layer prior to assembly of the inner layer into the multi-layer structure. Thus, in prior art methods components formed in an inner layer were subjected to the high temperatures of anneal bonding, or alternatively less preferred low temperature bonding processes had to be used.

The invention provides a method whereby the components are formed in an inner layer, typically, an inner silicon layer after the layers of the multi-layer structure have been bonded together. This is achieved in accordance with the method of claim 1 as follows.

In claim 1, the semiconductor device comprises three layers, typically, silicon layers, namely, a first layer, which is a bottom layer, a third layer, which is a top layer, and a second layer, which is an inner layer located between the bottom layer and the top layer. The component, such as a micro-mechanical component, is formed in the inner

layer. A first etch stop layer is located between the bottom layer and the inner layer, and a second etch stop layer is located between the top layer and the inner layer. The second etch stop layer is bonded to either the inner layer or the top layer, and typically, would be grown on the other of the inner and top layers. The layer to which the second etch stop layer is to be bonded is not important. It may be bonded to either the top or the inner layer, and thus would initially be grown on the other one of these two layers.

An essential step in the invention is the requirement that the second etch stop layer is patterned to define the component prior to the bonding of the second etch stop layer to the inner or top layer (to whichever it is to be bonded). The patterning of the second etch stop layer is carried out to facilitate etching of the component in the inner layer.

However, once the second etch stop layer has been patterned, and before the component is formed in the inner layer, the inner layer is then bonded to whichever of the inner and top layers to which it is to be bonded. It is only after bonding of all the layers to form the semiconductor structure that the component is formed in the inner layer. Since the second etch stop layer has already been patterned for facilitating etching of the component, the inner layer is etched through the top layer and the second etch stop layer to form the component.

In particular, the Examiner's attention is drawn to Fig. 9 of the drawings where the second etch stop layer 9 is illustrated as being patterned with openings 36 and portions 35, which define the micro-mechanical components (micro-mirrors 10) which are to be formed in the inner (intermediate) layer 5, and to Fig. 11 where a micro-mirror 10 is illustrated as having been formed in the inner (intermediate) layer 5 having been

etched through an opening 16 in the top layer 6, and in turn through the patterned second etch stop layer 9.

Thus, the layers of the semiconductor structure can be bonded together before the component in the inner layer is formed. Accordingly, the component is not subjected to the high temperatures of anneal bonding, since the component is formed after the anneal bonding process has been carried out.

The silicon layer to which the second etch stop layer is bonded is not important. The second etch stop layer can be grown on the inner layer and then bonded to the top layer or alternatively, the second etch stop layer can be grown on the top layer and then bonded to the inner silicon layer. What is important is that once the second etch stop layer has been grown on the layer on which it is to be grown, it should be patterned for facilitating subsequent etching of the component. Once the second etch stop layer is patterned for facilitating etching of the component and the layers of the semiconductor structure are bonded together, the top layer can then be etched down to the second etch stop layer, and further etching through the patterned second etch stop layer etches the component in the inner layer.

Accordingly, in claim 1 Applicants have claimed that "prior to bonding the second etch stop layer to the one of the second and third layers the second etch stop layer is patterned". This is to cover the possibility of the second etch stop layer being grown on either one of the second (inner) and third (top) layers and then bonded to the other of the second and third layers. After the second etch stop layer has been patterned, we then claim that it is bonded to the one of the second and third layers, in other words, the one of the second and third layers to which it is to be bonded. Applicants then claim that the

second layer is etched through the third layer and the second etch stop layer for forming the component in the second layer.

Contrary to the Examiner's interpretation of the specification set out in the second paragraph of Section 2 of the last official letter, it is respectfully submitted that the specification clearly discloses "prior to bonding the second etch stop layer to the one of the second and third layers, patterning the second etch stop layer to define the component in the second layer for facilitating etching of the second layer through the third layer".

Applicants would draw the Examiner's attention to the specification at page 3, line 2 to line 4. A similar form of words is used in the specification to describe a semiconductor device formed using the method at page 7, line 10 to line 14.

Turning now to Claims 12 and 34, it is respectfully submitted that claims 12 and 34 particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Claim 12 recites the first and second etch stop layers are grown layers. Claim 34 recites the first etch stop layer is a grown layer. The first and second etch stop layers are exactly as the terms imply, namely, etch stop layers. Whether the first and second etch stop layers are conductive or insulating layers is irrelevant to the invention, once they are etch stop layers. The specification at page 4, lines 9 and 10, and page 6, line 20 clearly provides a fair base for both Claims 12 and 34. At page 10, lines 15 and 16, where a non-limiting specific embodiment of the invention is being described, it is stated that the first and second etch stop layers are both oxide layers. At page 11, line 30 further elucidation of the first etch stop layer is provided where it is described as being "of oxide" "thermally grown". At page 12, line 13 further elucidation of the second etch stop layer is given where it is stated that it is "of oxide material" "thermally grown".

However, this is the description of a non-limiting example of the invention, see page 9, lines 19 to 21, and accordingly, is not to be considered as imposing any limitation on the claims.

In view of the foregoing comments, Applicants contend that all of the claims are now in full compliance with 35 USC §112. Accordingly, Applicants submit that all of the claims should now be in condition for allowance, and an early indication of same is respectfully requested.

Applicants' undersigned representative would like to suggest that a telephonic interview be held in order to expedite the prosecution of the application, and to avoid a possible appeal to the issues related to 35 USC §112.

Respectfully submitted,



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